THE DATASHEET OF

PESD5V0U1UT,215

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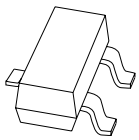

PESDxU1UT series

Ultra low capacitance ESD protection diode in SOT23 package

Rev. 02 — 20 August 2009 Product data sheet

1. Product profile

1.1 General description

Ultra low capacitance ElectroStatic Discharge (ESD) protection diode in a SOT23 (TO-236AB) small SMD plastic package designed to protect one high-speed data line from the damage caused by ESD and other transients.

1.2 Features

- Unidirectional ESD protection of one line
- Ultra low diode capacitance: C_d = 0.6 pF
- Max. peak pulse power: P_{PP} up to 200 W
- Low clamping voltage
- ESD protection > 23 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5; (surge)

1.3 Applications

- 10/100/1000 Ethernet
- FireWire
- Communication systems
- Local Area Network (LAN) equipment
- Computers and peripherals
- High-speed data lines

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse stand-off voltage					
	PESD3V3U1UT		-	-	3.3	V
	PESD5V0U1UT		-	-	5.0	V
	PESD12VU1UT		-	-	12	V
	PESD15VU1UT		-	-	15	V
	PESD24VU1UT		-	-	24	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V [1]	-	0.6	1.5	pF

[1] Measured from pin 1 to 2

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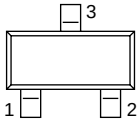
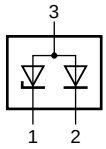
2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	cathode ESD protection diode		
2	cathode compensation diode		
3	common anode		

006aaa441

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD3V3U1UT	-	plastic surface mounted package; 3 leads	SOT23
PESD5V0U1UT			
PESD12VU1UT			
PESD15VU1UT			
PESD24VU1UT			

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD3V3U1UT	*AP
PESD5V0U1UT	*AQ
PESD12VU1UT	*AR
PESD15VU1UT	*AS
PESD24VU1UT	*AT

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

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5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{PP}	peak pulse power	8/20 µs	[1]			
	PESD3V3U1UT			-	80	W
	PESD5V0U1UT			-	80	W
	PESD12VU1UT			-	200	W
	PESD15VU1UT			-	200	W
	PESD24VU1UT			-	200	W
I_{PP}	peak pulse current	8/20 µs	[1]			
	PESD3V3U1UT			-	5	A
	PESD5V0U1UT			-	5	A
	PESD12VU1UT			-	5	A
	PESD15VU1UT			-	5	A
	PESD24VU1UT			-	3	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.

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Table 6. ESD maximum ratings

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]			
	PESD3V3U1UT			-	30	kV
	PESD5V0U1UT			-	30	kV
	PESD12VU1UT			-	30	kV
	PESD15VU1UT			-	30	kV
	PESD24VU1UT			-	23	kV
	PESDxU1UT	HBM MIL-STD-883		-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1 to 2

Table 7. ESD standards compliance

Standard	Conditions
IEC 61000-4-2; level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
HBM MIL-STD-883; class 3	> 4 kV

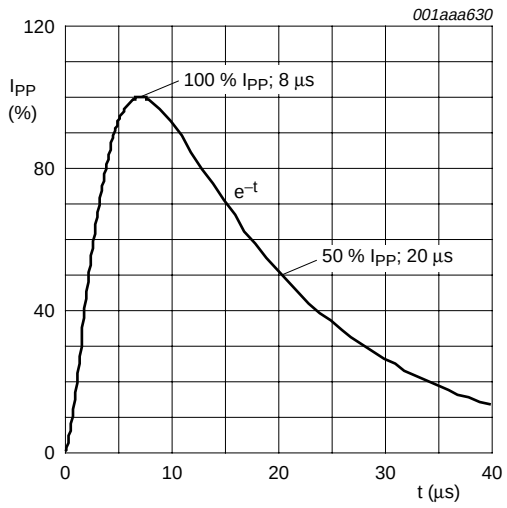

Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5

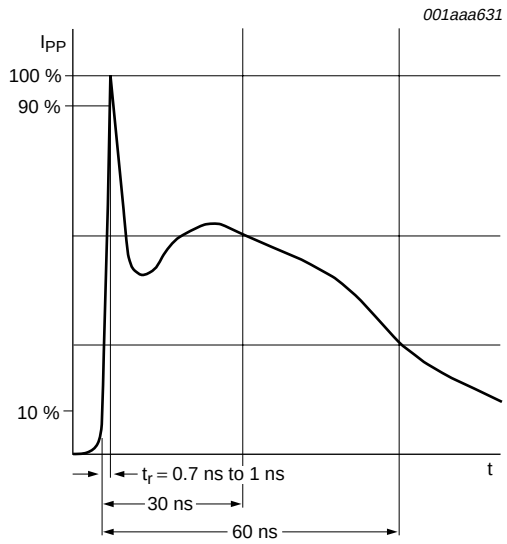

Fig 2. ESD pulse waveform according to IEC 61000-4-2

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6. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse stand-off voltage						
	PESD3V3U1UT			-	-	3.3	V
	PESD5V0U1UT			-	-	5.0	V
	PESD12VU1UT			-	-	12	V
	PESD15VU1UT			-	-	15	V
	PESD24VU1UT			-	-	24	V
I_{RM}	reverse leakage current						
	PESD3V3U1UT	V_{RWM} = 3.3 V		-	0.25	2	µA
	PESD5V0U1UT	V_{RWM} = 5.0 V		-	0.03	1	µA
	PESD12VU1UT	V_{RWM} = 12 V		-	< 1	50	nA
	PESD15VU1UT	V_{RWM} = 15 V		-	< 1	50	nA
	PESD24VU1UT	V_{RWM} = 24 V		-	< 1	50	nA
V_{BR}	breakdown voltage	I_R = 5 mA	[2]				
	PESD3V3U1UT			5.8	6.4	6.9	V
	PESD5V0U1UT			7.0	7.6	8.2	V
	PESD12VU1UT			14.2	15.0	16.7	V
	PESD15VU1UT			17.1	18.9	20.3	V
	PESD24VU1UT			25.4	27.8	30.3	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	[2]	-	0.6	1.5	pF
V_{CL}	clamping voltage		[1][2]				
	PESD3V3U1UT	I_{PP} = 1 A		-	-	9	V
		I_{PP} = 5 A		-	-	20	V
	PESD5V0U1UT	I_{PP} = 1 A		-	-	12	V
		I_{PP} = 5 A		-	-	21	V
	PESD12VU1UT	I_{PP} = 1 A		-	-	23	V
		I_{PP} = 5 A		-	-	39	V
	PESD15VU1UT	I_{PP} = 1 A		-	-	28	V
		I_{PP} = 5 A		-	-	53	V
	PESD24VU1UT	I_{PP} = 1 A		-	-	40	V
		I_{PP} = 3 A		-	-	76	V
r_{dif}	differential resistance	I_R = 1 mA					
	PESD3V3U1UT			-	-	400	Ω
	PESD5V0U1UT			-	-	80	Ω
	PESD12VU1UT			-	-	200	Ω
	PESD15VU1UT			-	-	225	Ω
	PESD24VU1UT			-	-	300	Ω

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1 to 2

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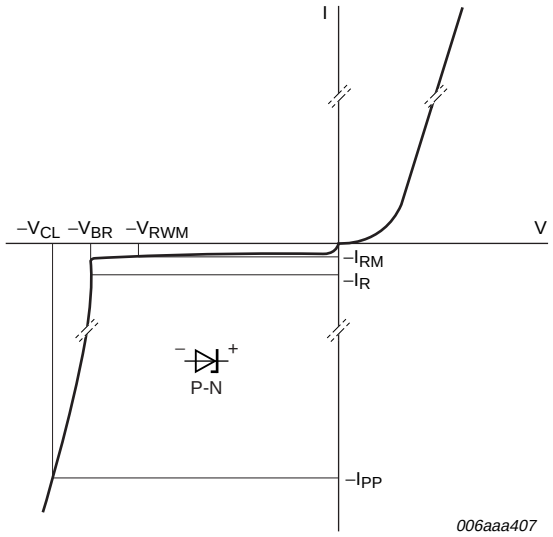
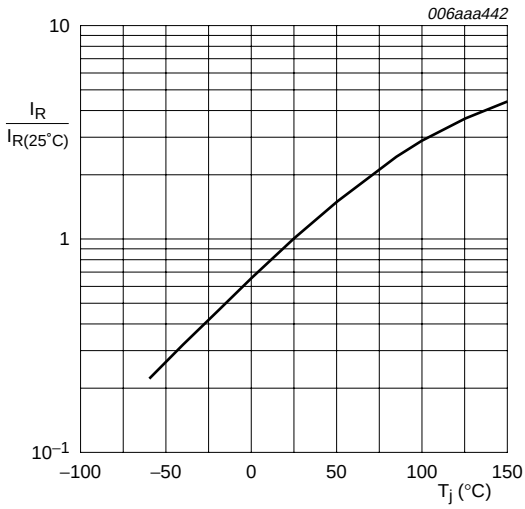


Fig 3. V-I characteristics



PESD3V3U1UT; PESD5V0U1UT

I_R is less than 10 nA at 150 °C for:

PESD12VU1UT; PESD15VU1UT; PESD24VU1UT

Fig 4. Relative variation of reverse leakage current as a function of junction temperature; typical values

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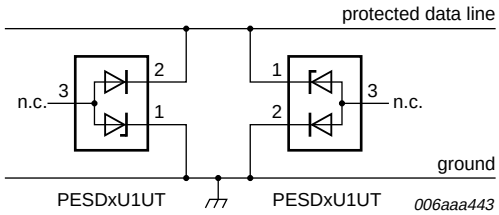
7. Application information

The PESDxU1UT series is designed for protection of high-speed datalines from damage caused by ESD and surge pulses. PESDxU1UT devices combine an ESD protection diode and an ultra low capacitance compensation diode to ensure an effective device capacitance as low as 0.6 pF. The PESDxU1UT series provides a surge capability of up to 200 W per line for an 8/20 µs waveform.



Two PESDxU1UT devices in anti-parallel configuration provide ESD protection in a common-mode application.

The two PESDxU1UT devices should be connected as follows:

protected data line is connected to

device 1 / pin 2

device 2 / pin 1

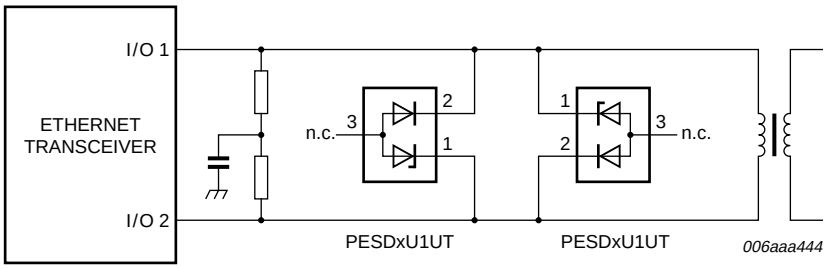
Ground is connected to

device 1 / pin 1

device 2 / pin 2

pin 3 is not connected for both devices

Fig 5. Bidirectional ESD protection of one line, common mode



Two PESDxU1UT devices in anti-parallel configuration provide ESD protection in a differential-mode configuration as e.g. for Ethernet applications.

The two PESDxU1UT should be connected as follows:

I/O line 1 is connected to

device 1 / pin 2

device 2 / pin 1

I/O line 2 is connected to

device 1 / pin 1

device 2 / pin 2

pin 3 is not connected for both devices

Fig 6. Differential mode Ethernet protection

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Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PESDxU1UT as close to the input terminal or connector as possible.
2. The path length between the PESDxU1UT and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all printed-circuit board conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer printed-circuit boards, use ground vias.

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8. Test information

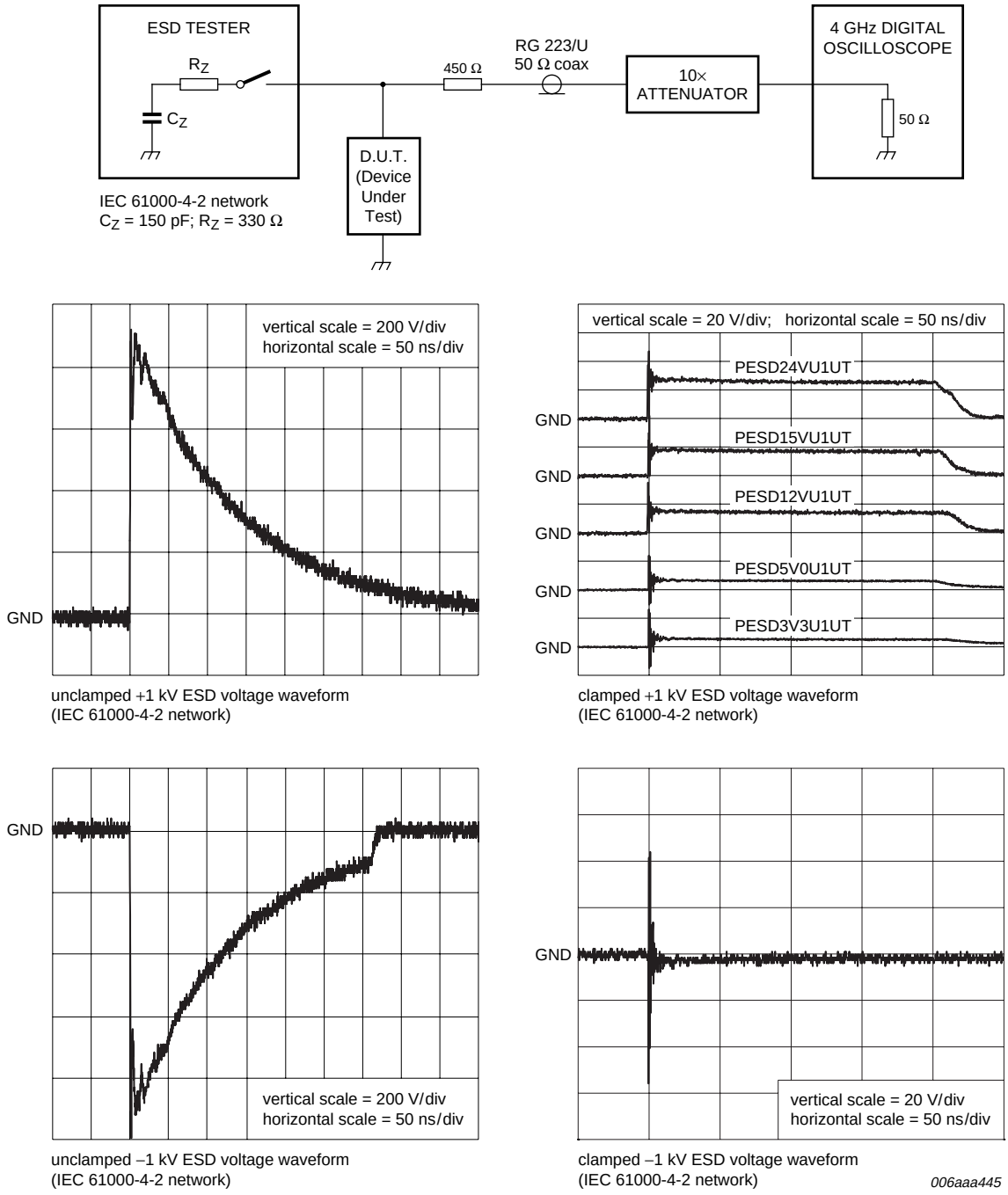

Fig 7. ESD clamping test setup and waveforms

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9. Package outline

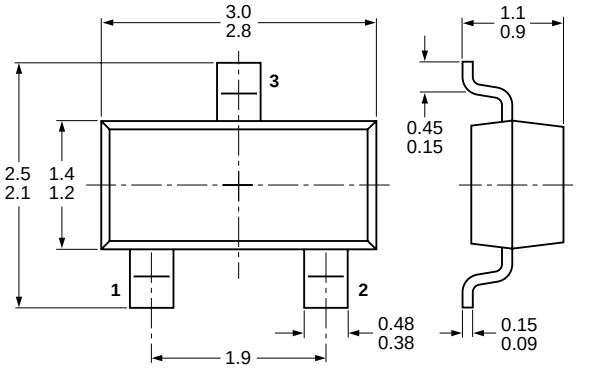

Fig 8. Package outline SOT23 (TO-236AB)

10. Packing information

Table 9. Packing methods

The -xxx numbers are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PESD3V3U1UT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-235
PESD5V0U1UT				
PESD12VU1UT				
PESD15VU1UT				
PESD24VU1UT				

[1] For further information and the availability of packing methods, see Section 13.

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11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESDXU1UT_SER_2	20090820	Product data sheet	-	PESDXU1UT_SER_1
Modifications:	• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.			
PESDXU1UT_SER_1	20050511	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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